

What is claimed is:

Sub 317
1 1. In a communication arrangement having analog circuitry and having digital signal
2 processing circuitry clocked sufficiently fast to generate noise, the analog circuitry
3 susceptible to processing corrupted data due to the noise coupled thereto, a method for
4 reducing noise passed from the digital signal processing circuitry, comprising the steps
5 of:

6 using the analog circuitry to capture information data from an incoming stream for
7 at a first time interval while the digital signal processing circuitry is in a reduced-activity
8 mode; and

9 in a mode other than the reduced-activity mode and during a second shorter time
10 interval, clocking the digital signal processing circuitry to permit digital signal processing
11 of the captured information data.

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1 2. A method for reducing noise passed from the digital signal processing circuitry,
2 according to claim 1, wherein the step of effectively disabling the processing of data by
3 the analog circuitry while processing the data with the digital signal processing circuitry
4 occurs during a known guard time for the data being communicated to the
5 communication arrangement.

Sub 317
1 3. A method for reducing noise passed from the digital signal processing circuitry,
2 according to claim 2, further including the step of providing both the analog circuitry and
3 the digital signal processing circuitry on the same chip, and wherein the step of using the

4 analog circuitry to process data includes receiving the data in the form of low-energy
5 data.

1 4. A method for reducing noise passed from the digital signal processing circuitry,
2 according to claim 2, wherein the step of using the analog circuitry to process data
3 includes receiving the data in the form of low-energy data and storing the data in a
4 memory circuit.

1 5. A method for reducing noise passed from the digital signal processing circuitry,
2 according to claim 4, further including inhibiting the analog circuitry from storing data in
3 a memory circuit.

1 6. A method for reducing noise passed from the digital signal processing circuitry,
2 according to claim 1, further including at least reducing power to at least one of the
3 analog circuitry and the digital circuitry while the other circuitry is processing data.

1 7. A method for reducing noise passed from the digital signal processing circuitry,
2 according to claim 1, wherein the first data-communication interval is substantially
3 greater than the second data-communication interval.

1 8. A method for reducing noise passed from the digital signal processing circuitry,
2 according to claim 1, further including providing a memory circuit in which data is

3 written into the memory circuit at a rate that is asynchronous to the rate at which data is
4 read out from the memory circuit.

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1 9. A method for reducing noise passed from the digital signal processing circuitry,
2 according to claim 1, further including the steps of: providing a memory circuit coupled
3 for access by at least a portion of the analog circuitry and by at least a portion of the
4 digital signal processing circuitry; using said at least a portion of the analog circuitry to
5 read data out of the memory circuit and using said at least a portion of the digital signal
6 processing circuitry to write data into the memory circuit.

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1 10. A method for reducing noise passed from the digital signal processing circuitry,
2 according to claim 1, further including the steps of: providing a memory circuit coupled
3 for access by at least a portion of the analog circuitry and by at least a portion of the
4 digital signal processing circuitry; using said at least a portion of the analog circuitry to
5 write data into the memory circuit and using said at least a portion of the digital signal
6 processing circuitry to read data out of the memory circuit.

Sub C1
1 11. A communication arrangement having analog circuitry and digital signal
2 processing circuitry, the analog circuitry susceptible to processing corrupted data due to
3 noise coupled thereto via digital signal processing circuitry, an arrangement for reducing
4 noise passed from the digital signal processing circuitry, comprising:

1 16. A communication arrangement, according to claim 11, wherein the means for
2 using the analog circuitry to process data while the digital signal processing circuitry is in
3 a reduced activity mode includes means for receiving low-energy, high-frequency data.

1 17. A communication arrangement, according to claim 11, wherein the means for
2 using the analog circuitry to process data while the digital signal processing circuitry is in
3 a reduced activity mode includes means for transmitting data.

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1 18. A communication arrangement susceptible to processing corrupted data due to
2 noise coupled thereto via high-speed data processing, comprising:
3 a chip including both digital signal processing circuitry and analog circuitry, the
4 digital signal processing circuitry having a reduced activity mode and a high-speed data
5 processing mode, and the analog circuitry configured and arranged to process data during
6 a first data-communication interval while the digital signal processing circuitry is in the
7 reduced activity mode; and
8 means for effectively disabling the processing of data by the analog circuitry
9 during a second shorter data-communication interval while processing the data with the
10 digital signal processing circuitry.

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1 19. A communication arrangement, according to claim 18, wherein the chip further
2 includes the means for effectively disabling the processing of data.

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1 20. A communication arrangement, according to claim 18, wherein digital signal
2 processing circuitry and analog circuitry are configured and arranged to receive data.

1 21. A communication arrangement, according to claim 18, wherein digital signal
2 processing circuitry and analog circuitry are configured and arranged to receive and
3 transmit data.

1 22. A communication arrangement, according to claim 18, wherein both digital signal
2 processing circuitry and analog circuitry are configured and arranged to transmit data.

1 23. In a communication arrangement having analog circuitry and digital signal
2 processing circuitry, the analog circuitry coupled to receive streams of data presented
3 thereto in the form of high-frequency signals for subsequent processing by the digital
4 signal processing circuitry, a method for reducing noise passed from the digital signal
5 processing circuitry to the data, comprising the steps of:

6 using the analog circuitry to process and to store the data during a first data-
7 communication interval while the digital signal processing circuitry is in a reduced
8 activity mode; and

9 disregarding additional data in the streams of data presented to the analog
10 circuitry during a second shorter data-communication interval while processing the stored
11 data with the digital signal processing circuitry.

1 24. In a communication arrangement having analog circuitry and digital signal
2 processing circuitry, the analog circuitry coupled to receive streams of data presented
3 thereto in the form of high-frequency signals for subsequent processing by the digital
4 signal processing circuitry, a method for reducing noise passed from the digital signal
5 processing circuitry to the data, comprising the steps of:

6 using the analog circuitry to process and to store the data during a first data-
7 communication interval while the digital signal processing circuitry is in a reduced
8 activity mode; and

9 disregarding additional data in the streams of data presented to the analog
10 circuitry during a second shorter data communication interval while processing the stored
11 data with the digital signal processing circuitry.

1/ 25. A communication arrangement susceptible to processing corrupted data due to
2 noise coupled thereto by high-speed data processing, comprising:

3 a chip including both digital signal processing circuitry and analog circuitry, the
4 digital signal processing circuitry having a reduced activity mode and a high-speed data
5 processing mode, and the analog circuitry configured and arranged to process data during
6 a first data-communication interval while the digital signal processing circuitry is in the
7 reduced activity mode; and

8 means for effectively disabling the processing of data by the analog circuitry
9 during a second shorter data-communication interval while processing the data with the
10 digital signal processing circuitry.

